LISTING OF THE CLAIMS

The following Listing of the Claims replaces all prior listings of the claims within this application.

Claim 13 is amended.

1. (previously presented) A method for fabricating a microelectronic fabrication comprising:

providing a substrate;

forming over the substrate a series of patterned conductor layers separated by a series of dielectric layers; and

forming over the substrate in electrical connection with the series of patterned conductor layers separated by the series of dielectric layers at least one fuse layer formed simultaneously with an alignment mark, wherein the at least one fuse layer is formed at a level no lower than a highest of the series of patterned conductor layers and wherein the at least one fuse layer and the highest of the series of patterned conductor layers are formed of different conductor materials.

2. (original) The method of claim 1 wherein the microelectronic fabrication is selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

3. (original) The method of claim 1 wherein the at least one fuse layer is formed simultaneously with a bond pad layer within the microelectronic fabrication.

4. – 5. (canceled)

6. (original) The method of claim 1 wherein the at least one fuse layer is formed of an aluminum containing conductor material and the highest of the series of patterned conductor layers is formed of a copper containing conductor material.

7. - 12. (canceled)

13. (currently amended) A method for fabricating a microelectronic fabrication comprising:

providing a substrate;

forming over the substrate a series of patterned conductor layers separated by a series of dielectric layers; and

forming over the substrate in electrical connection with the series of patterned conductor layers separated by the series of dielectric layers at least one fuse layer, wherein the at least one fuse layer is formed at a level no lower than a highest of the series of patterned conductor layers and wherein the at least one fuse layer is formed simultaneously with an alignment mark and a bond pad within the microelectronic fabrication.